CMOS Compatible 3D Integrated Memristive Memory Array

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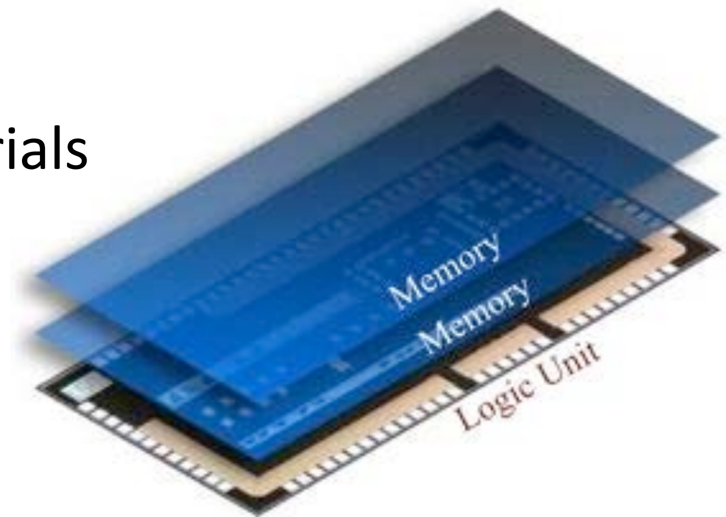
Why ReRAMs?

- **ReRAM characteristics:**
  - <u>CMOS BEoL compatible</u> : T°, materials
  - <u>Compact cell structure</u> : $4F^2$
  - <u>Low operating voltage</u> : <2V
  - <u>Low cost</u> : 3 or less mask process

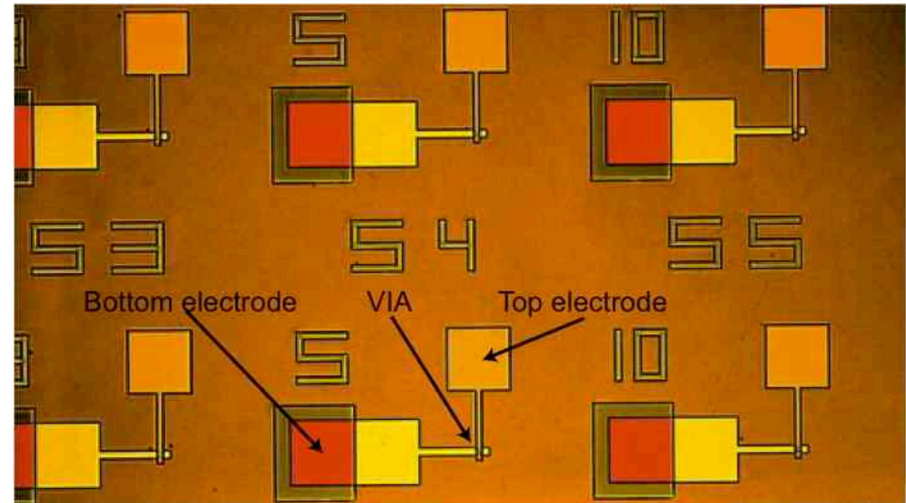


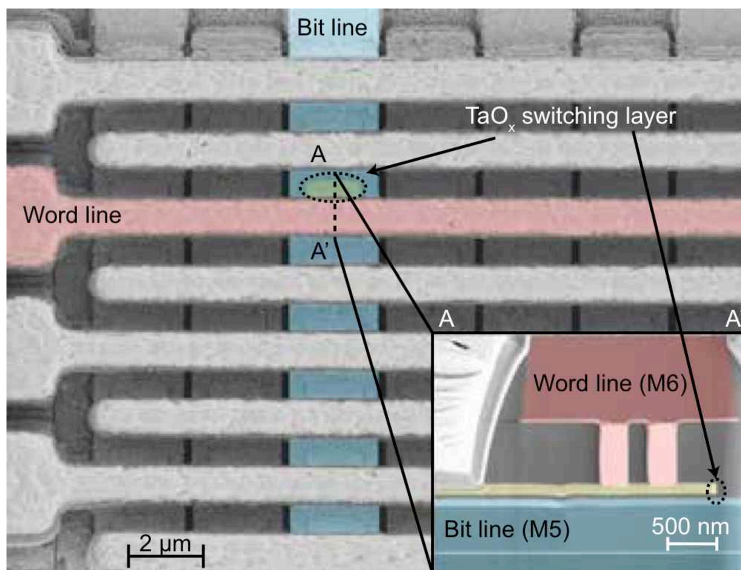
- **ReRAM application areas:**
  - Embedded non-volatile memories
  - 3D high density memories
  - Neuromorphic circuits

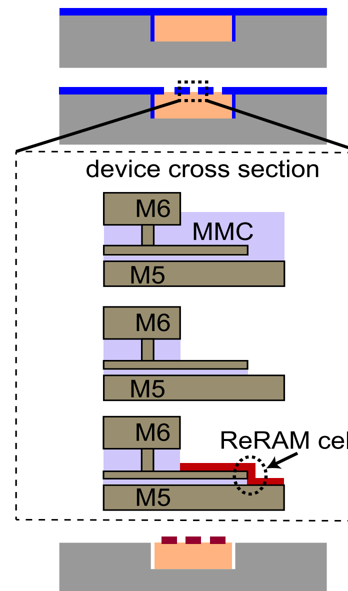
Image: wellcomeimages.com

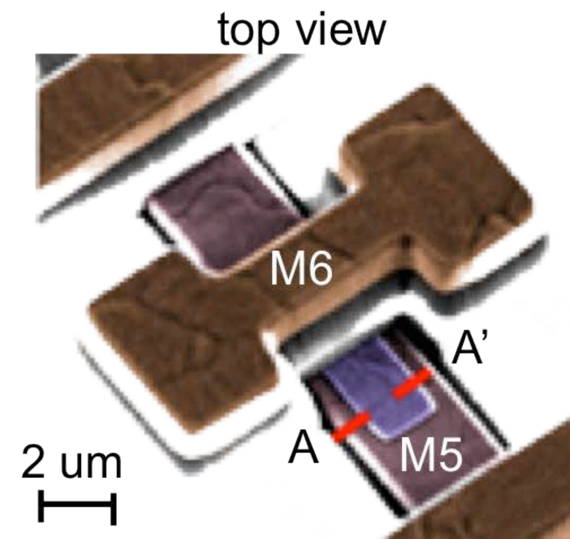
Fabricated devices @ EPFL

- **Wafer-based processing**
- **10um to 40nm ReRAMs**
  - Pt or TiN bottom electrode
  - LTO or SiN passivation
  - HfOx / TaOx / WOx based
  - TiN top electrode



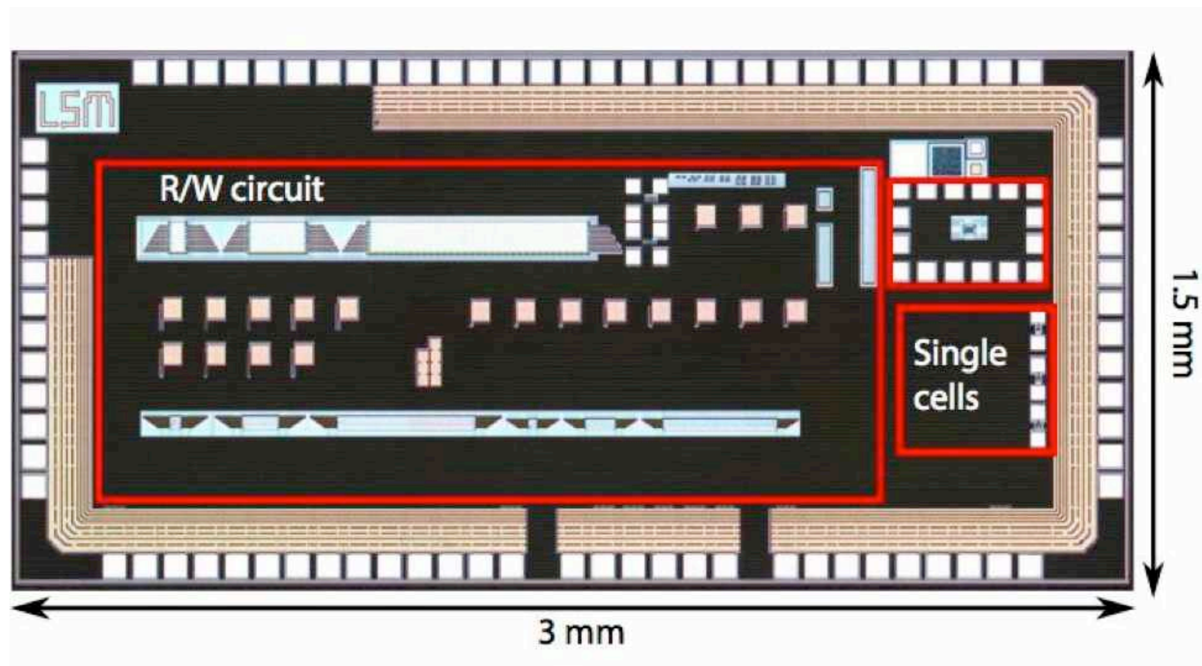


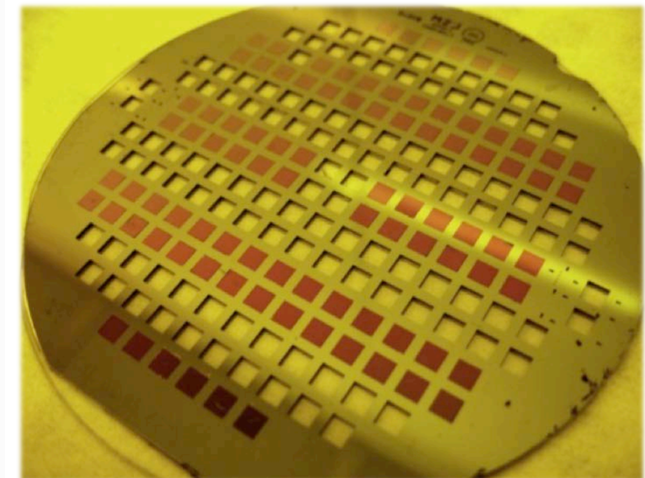




Chip level integration: crossbar arrays

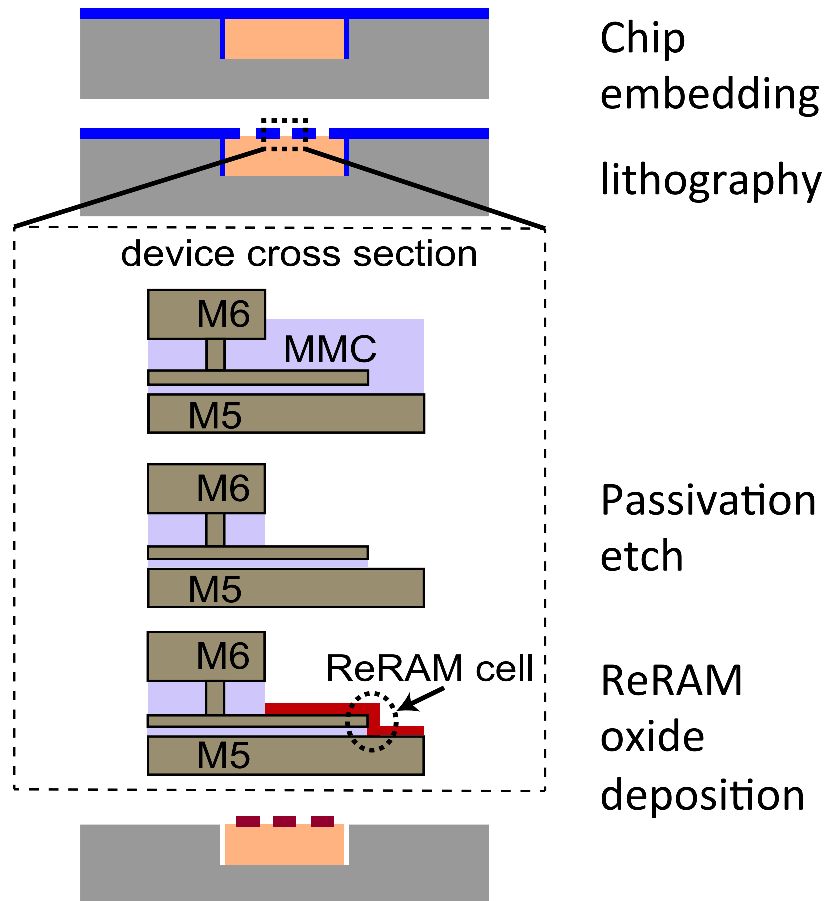
- Advantages: low cost, fast prototyping ability
- Challenges: process single CMOS chips
- Standard CMOS technology (180nm and lower)
- Predisposed for ReRAM crossbars BEoL integration @ EPFL
- Read/Write circuit on the front-end

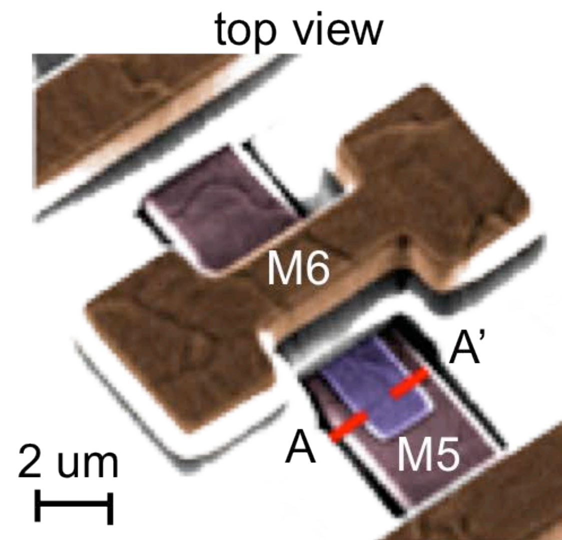




ReRAM-CMOS integration - MMC

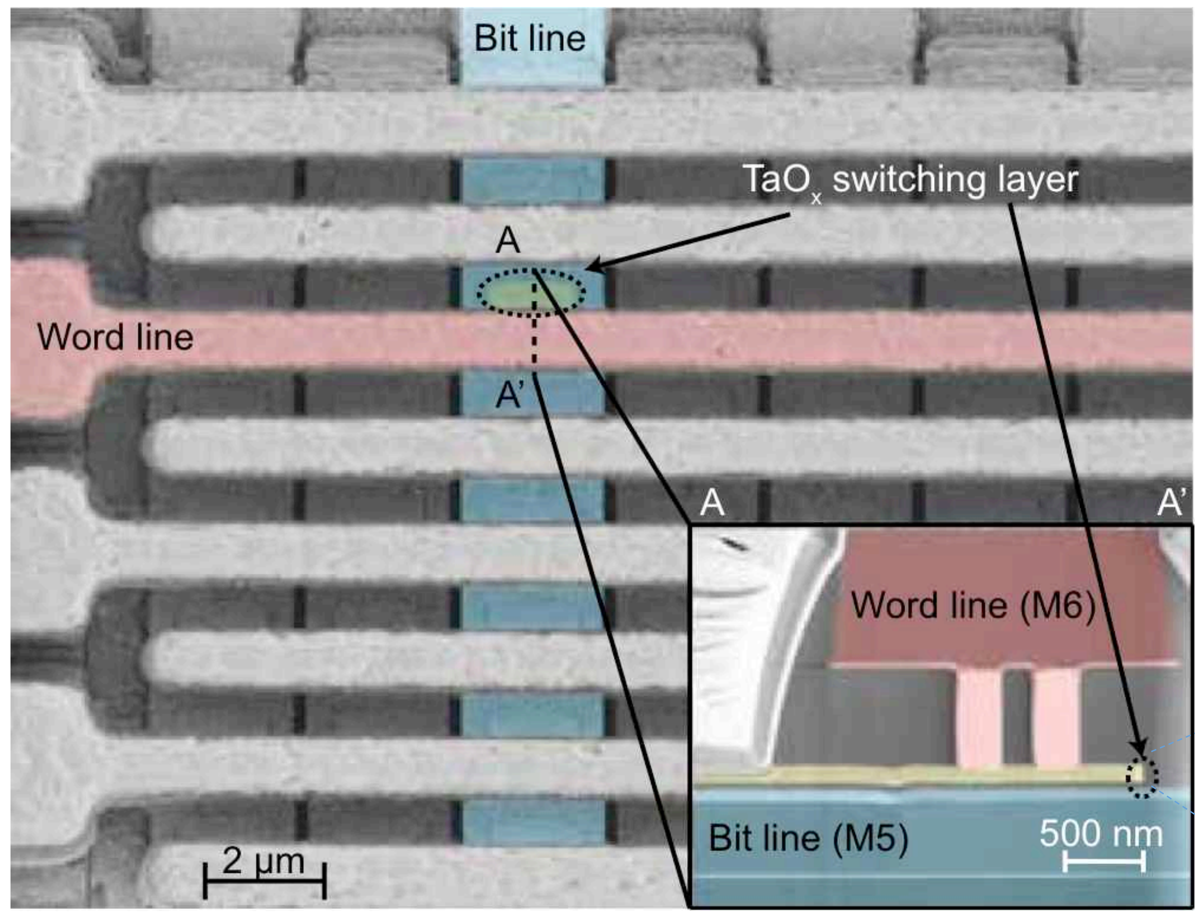
- **MMC based: metal-to-metal capacitor**
- **No need for additional high resolution lithography steps**

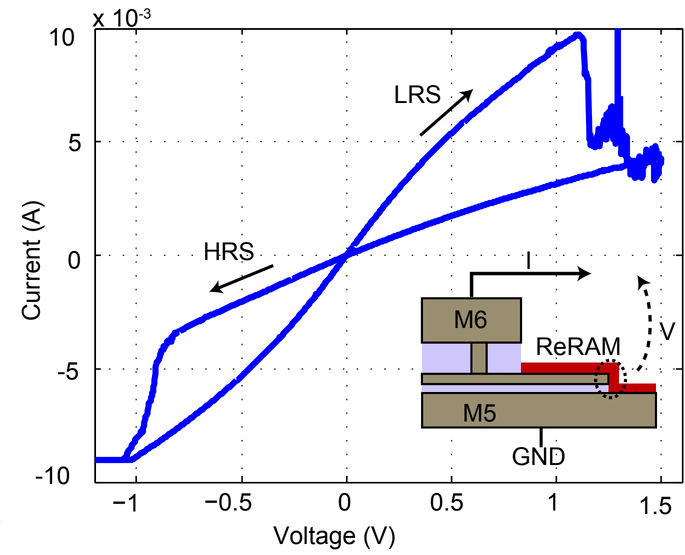


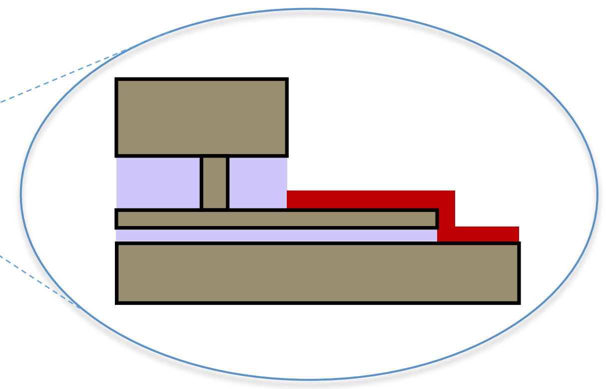


MMC detail

ReRAM integrated devices







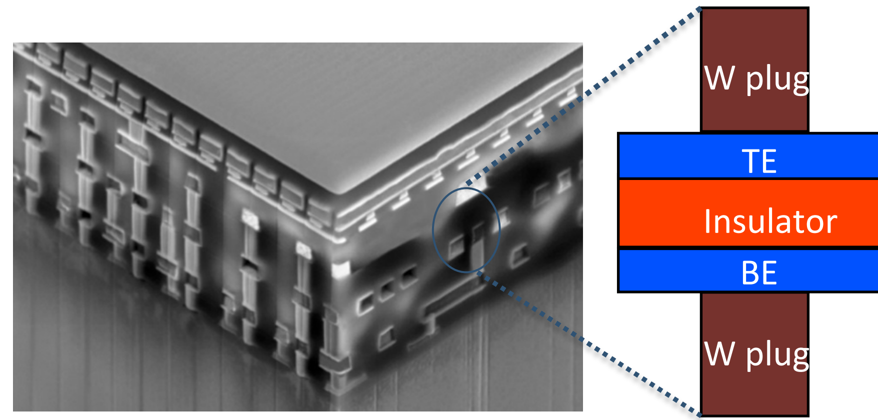
TiN/TaOx/TiN forming-free, Vset = -1V, Vreset = 1.3V

Sandrini, Microelectr. Eng. 2015

Using Tungsten (W) Vias in the BEoL Metal Stack

ReRAM CMOS co-integration

- ReRAM Fabrication BEOL CMOS compatibility
- High density with small size



Wafer scale challenges

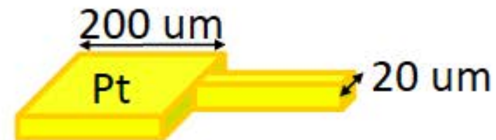
- Low accessibility
- High fabrication cost
- Need for nm-scale photolithography

Chip-level ReRAM-CMOS co-integration

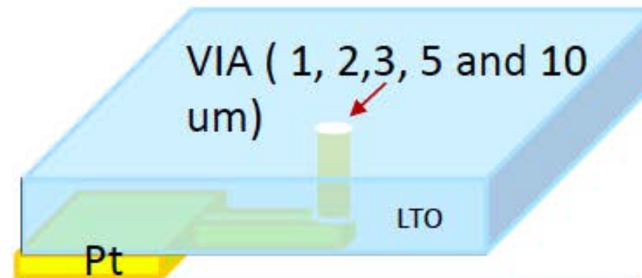
Single cell ReRAM

Fabrication

1) Ti/Pt BE patterning



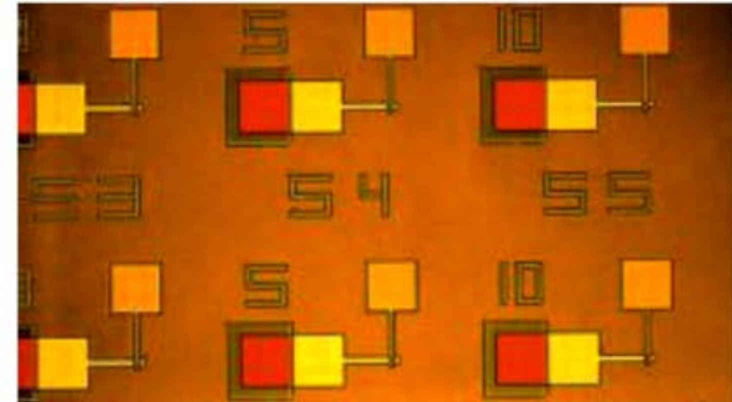
2) LTO via patterning



3) WOx deposition

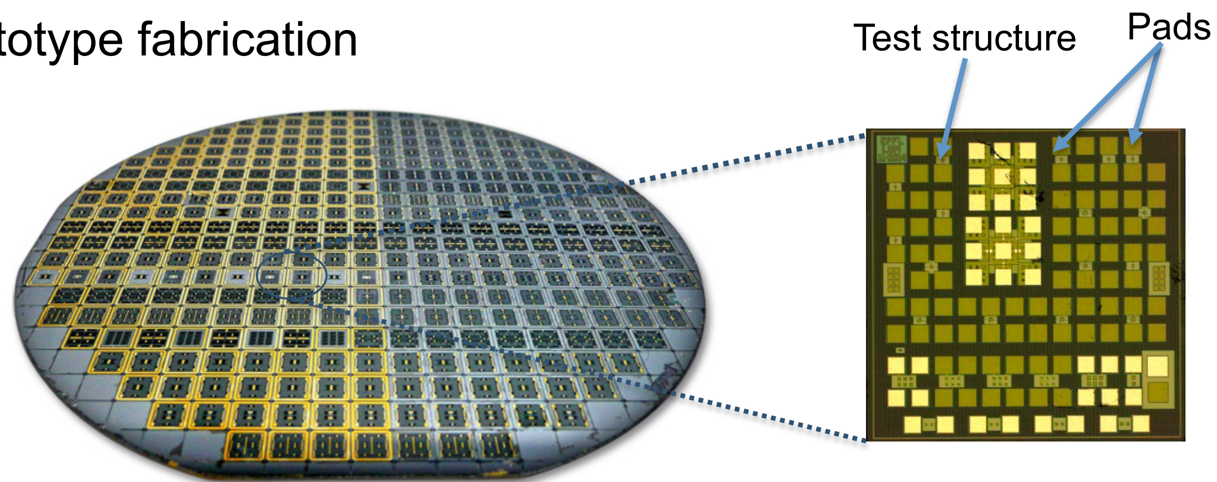
4) TiN TE pattering

Top view of final device



- **BE**: Pt, easy process
- **Re**: WOx, comparable to integrated memory
- **LTO** : low dielectric constant
- **TE** : TiN, good electrical characterization

- **Chip-level ReRAM-CMOS co-integration**
- **1kb passive ReRAM array on fully finished CMOS chip**
  - High design flexibility
  - Well established CMOS technology
  - Low fabrication cost
  - Easy prototype fabrication



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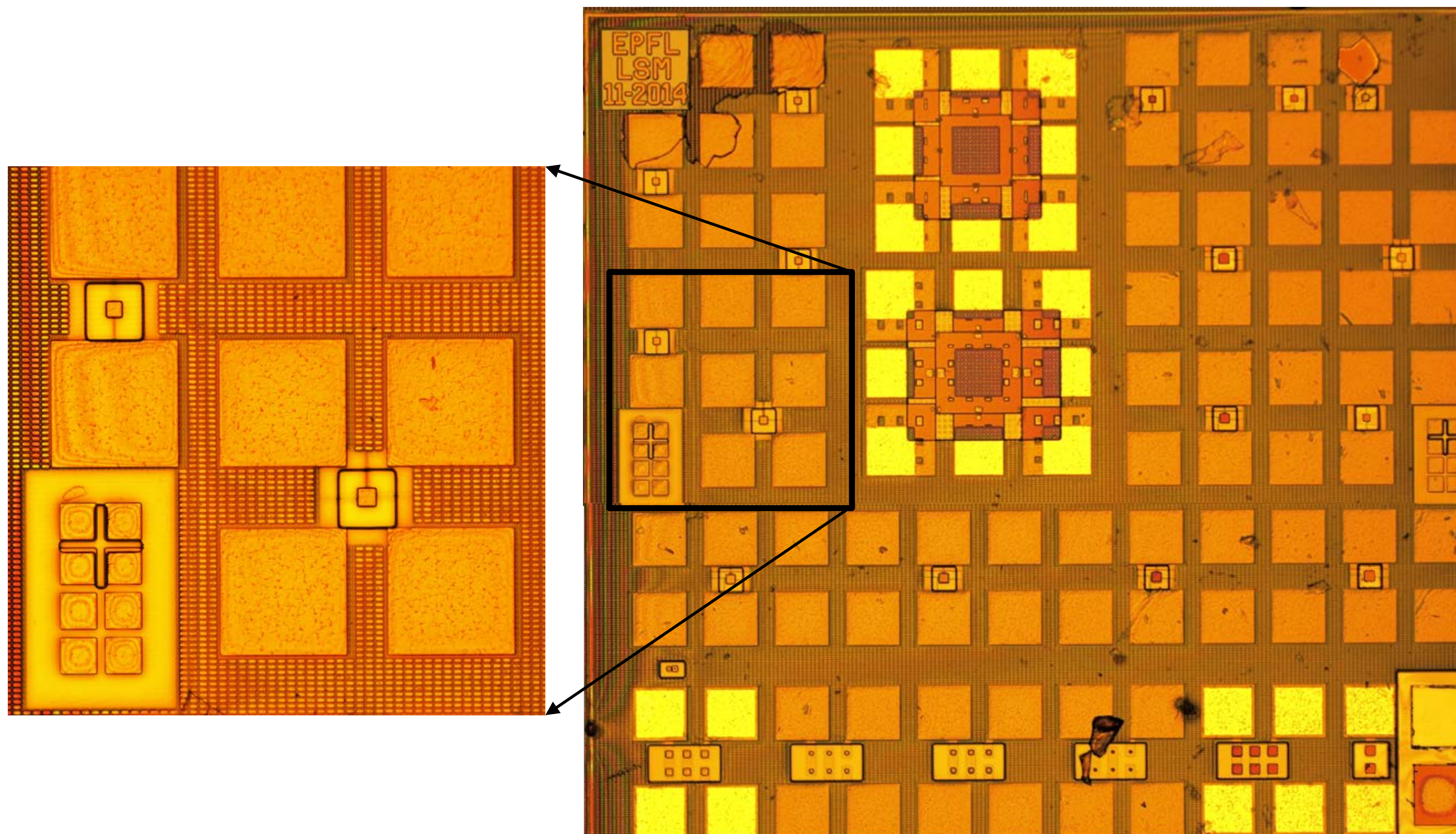
- After Al etch, STS , Perfect alignment



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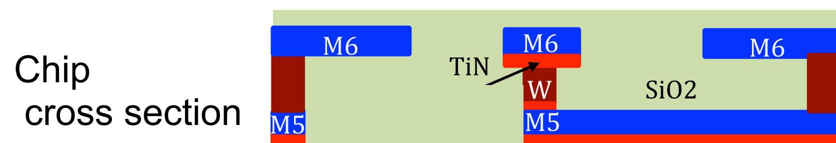
ReRAM-CMOS co-integration

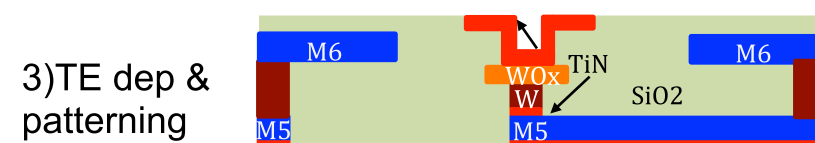
Chip cross section



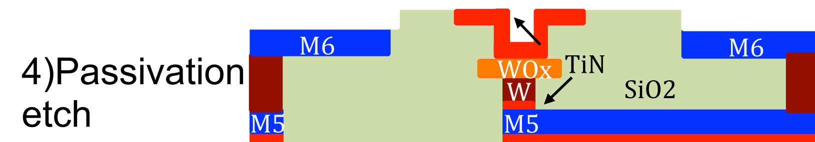
1)lithography & etching

2)RTP

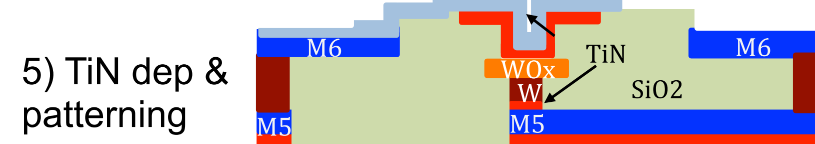
3)TE dep & patterning



4)Passivation etch



5) TiN dep & patterning



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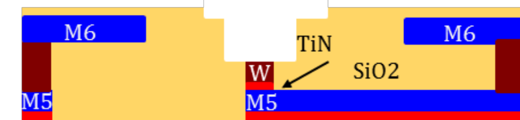
Co-integration (via based)-WOx

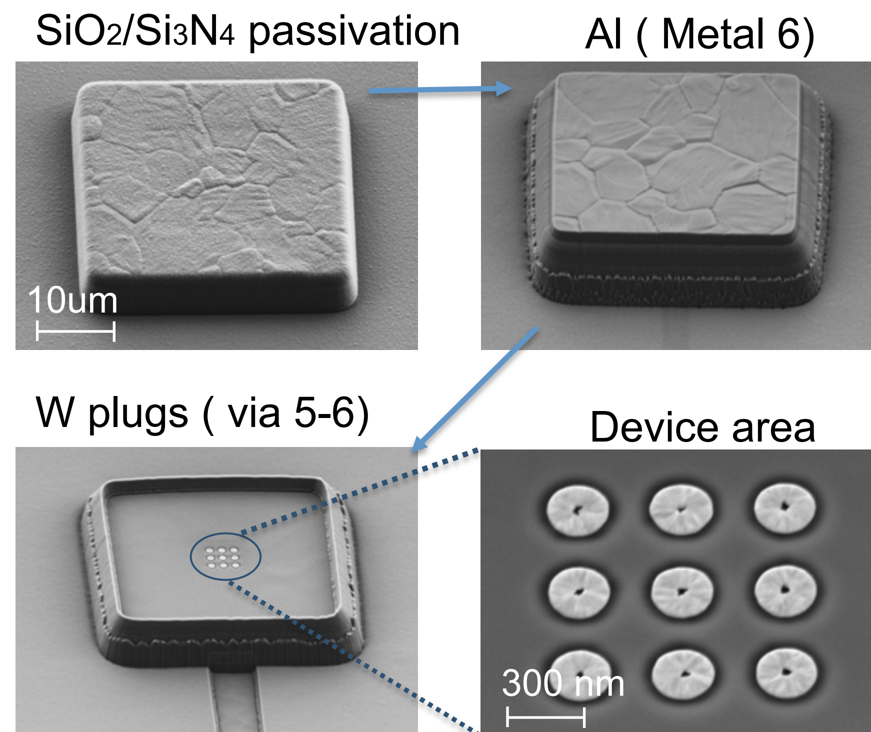
ReRAM-CMOS co-integration

1) lithography & etching



❑ **RIE (Chemistry: CF4, BCl3/Cl2, SF6)**

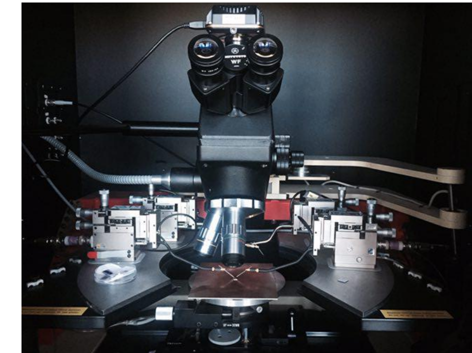
- Chip alignment
- Precise etching depth (EPD)
- Etching temperature (CMOS BEOL compatibility)
- Good selectivity



Single cell ReRAM (WOx)

Electrical characterization

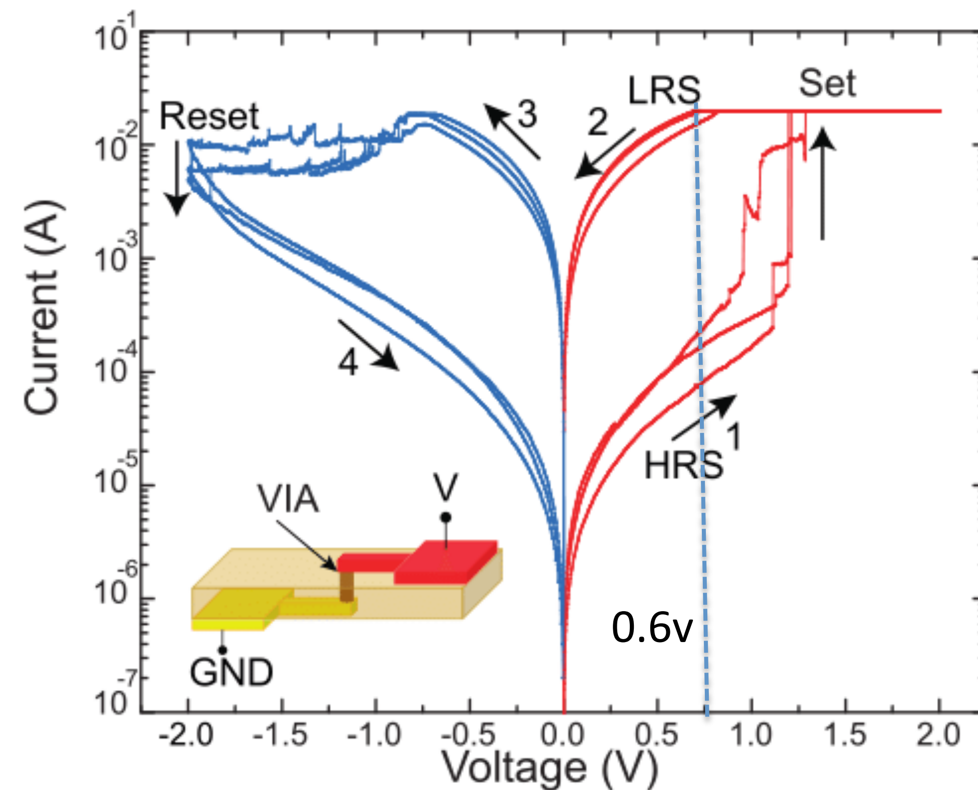
- Parameter analyzer (Agilent B1500)



- Current compliance: **10 mA**
- Set : at 1.2**V** & **10 mA**
- Reset : at **-1.8V** & **1 mA**

- **Bipolar** switching mechanism
- HRS : **90 kΩ**
  LRS : **30 Ω**

- **Relatively low voltage** operation



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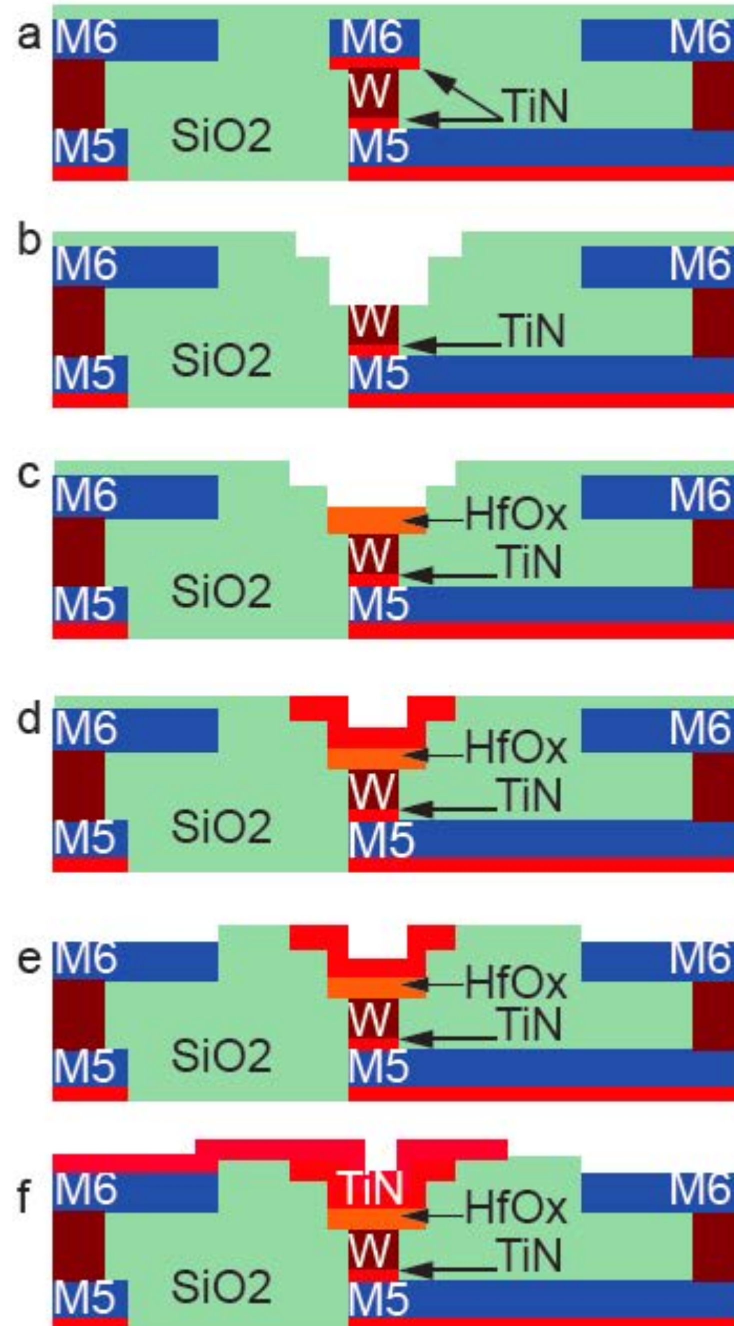
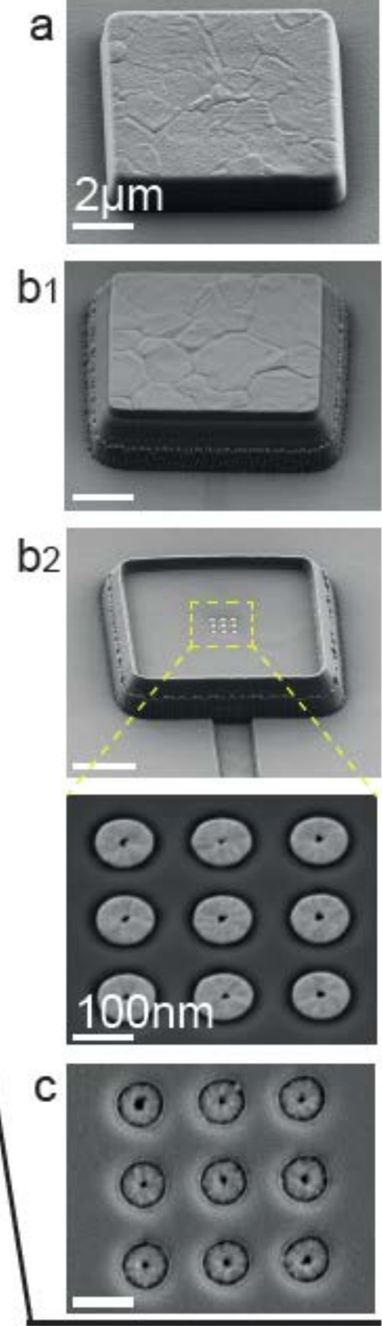
HfOx deposition on W (Tungsten) via





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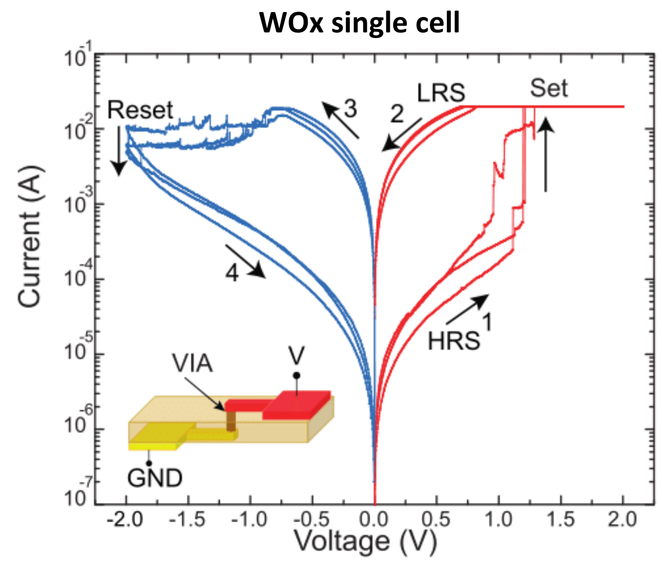
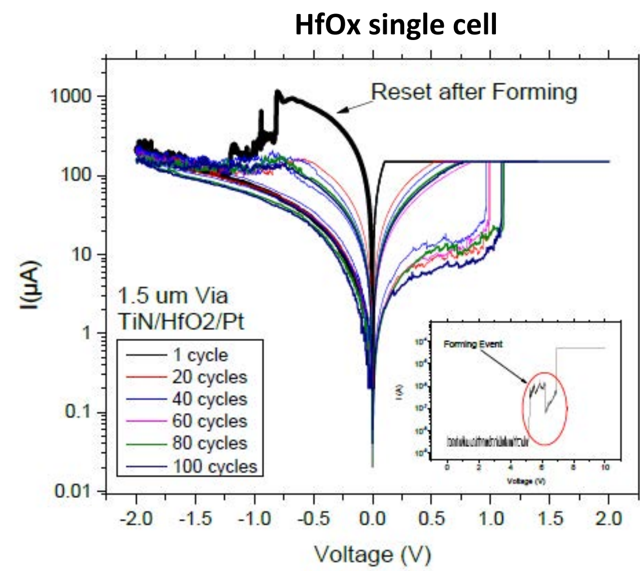
Electrical characterization HfOx and WOx ReRAM integration

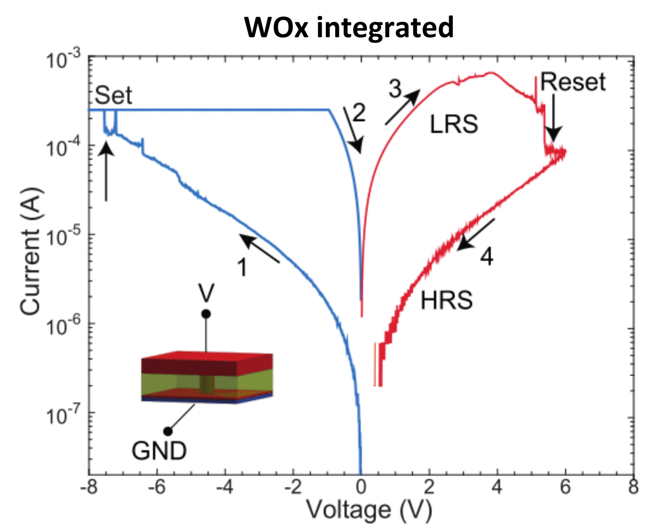
WOx single cell



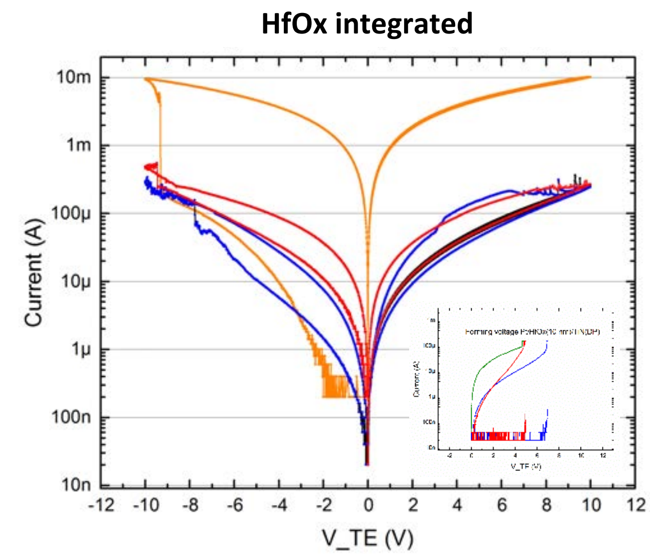
HfOx single cell



WOx integrated



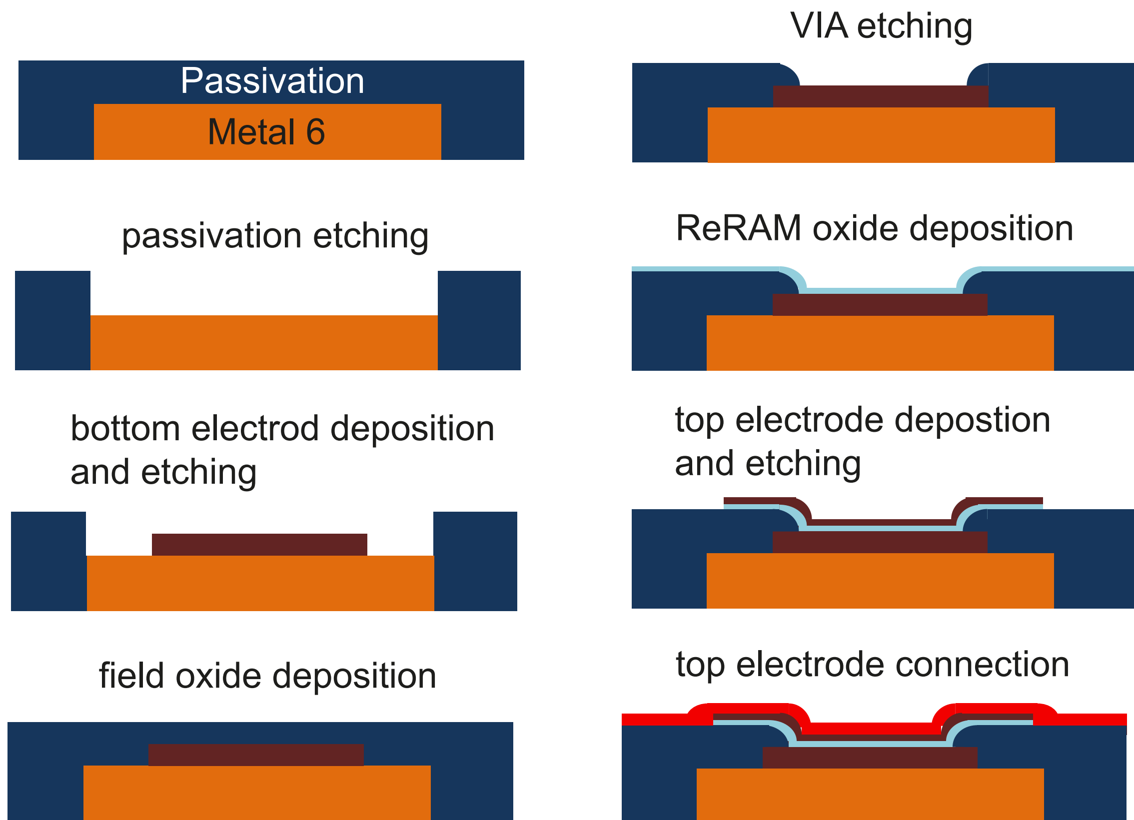
HfOx integrated



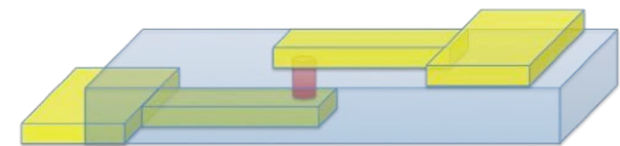
ReRAM-CMOS integration – Metal 5/6 process

- **Reproduce the process flow for the single ReRAM cells on the chip BEoL**

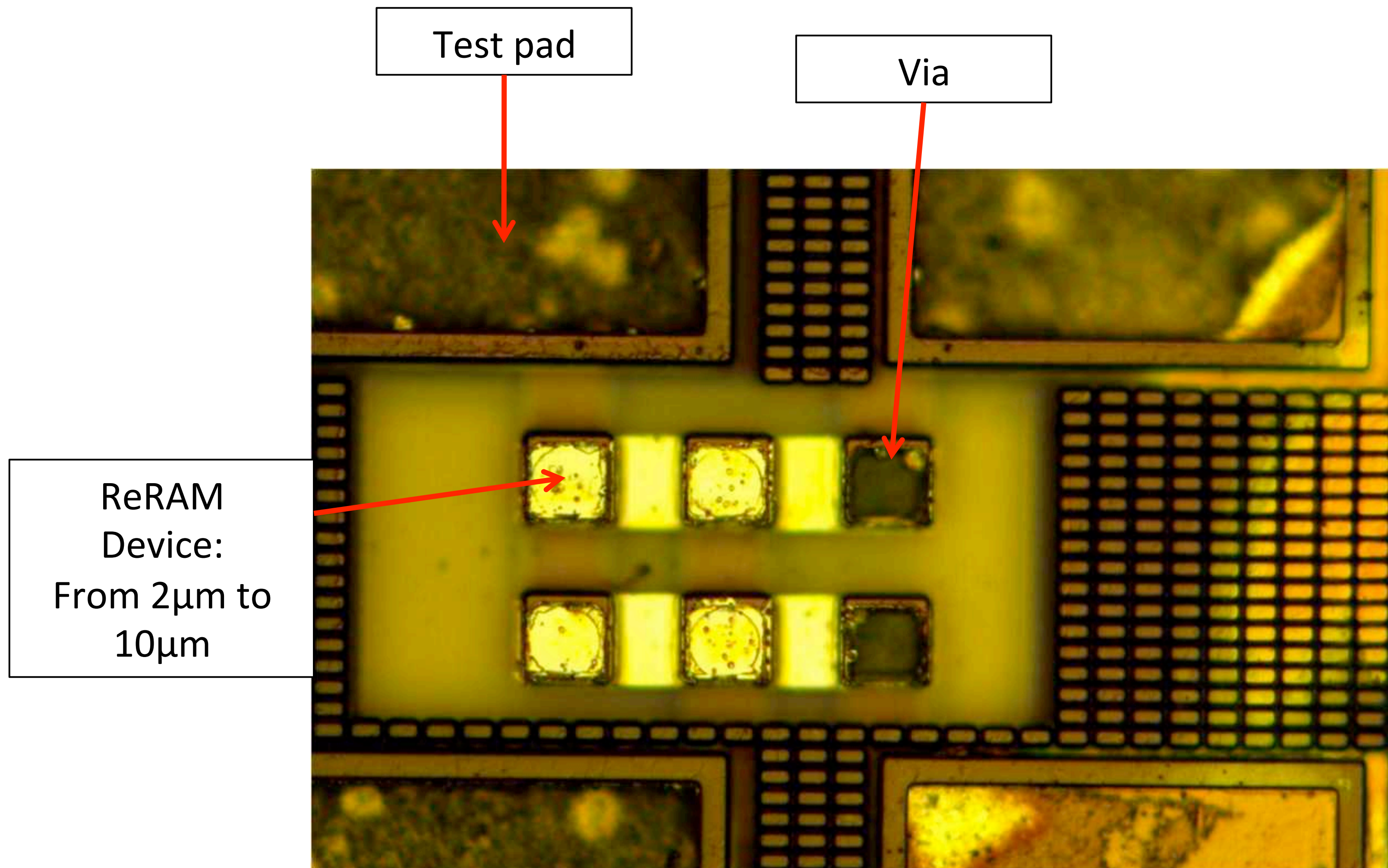
Process flow



Wafer based devices



ReRAM integrated devices



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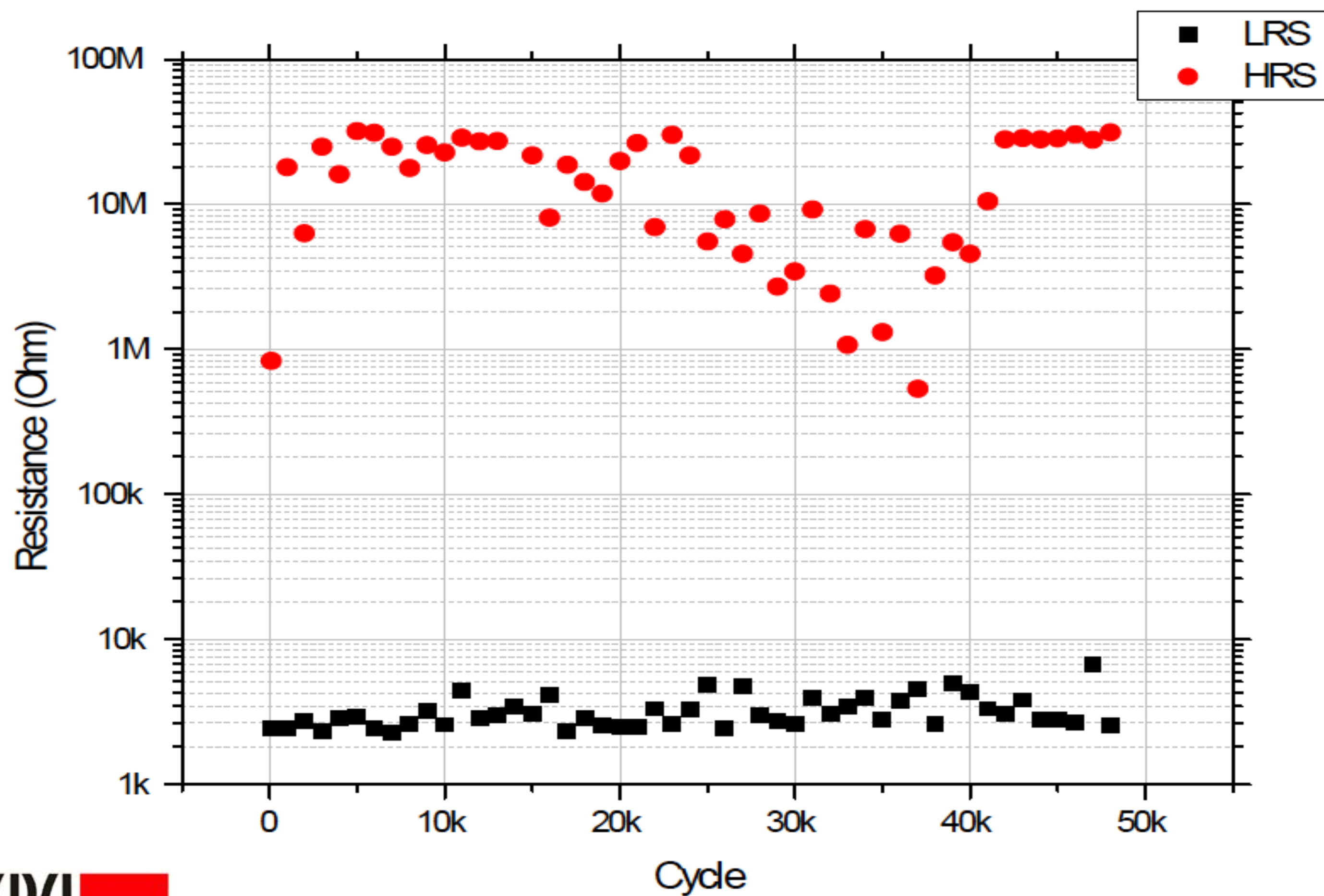
Endurance

Pt/HfOx(5nm)/Ti(3nm)/TiN - LTO passivation



Vreset = - 2.25 V

Vset = + 1.15 V

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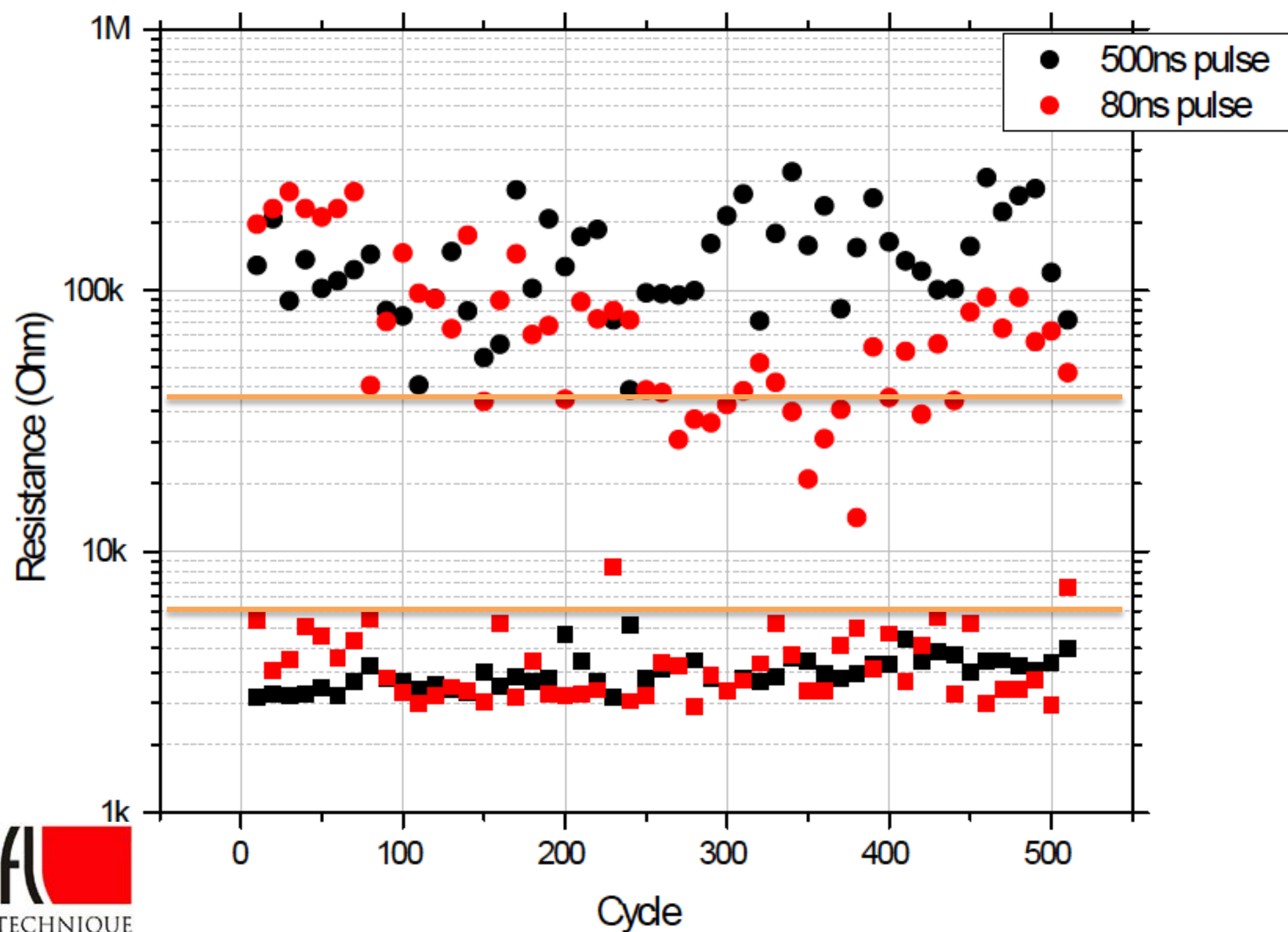
Pulse speed influence

Pt/HfOx(5nm)/Ti(3nm)/TiN - SiN passivation / ion beam etching

Pulses: Set 1.4V, Reset -1.8V, 20% pulse rise time, gate voltage 1.9V (180uA)



Vreset = - 1.75 V
Vset = + 1.25 V

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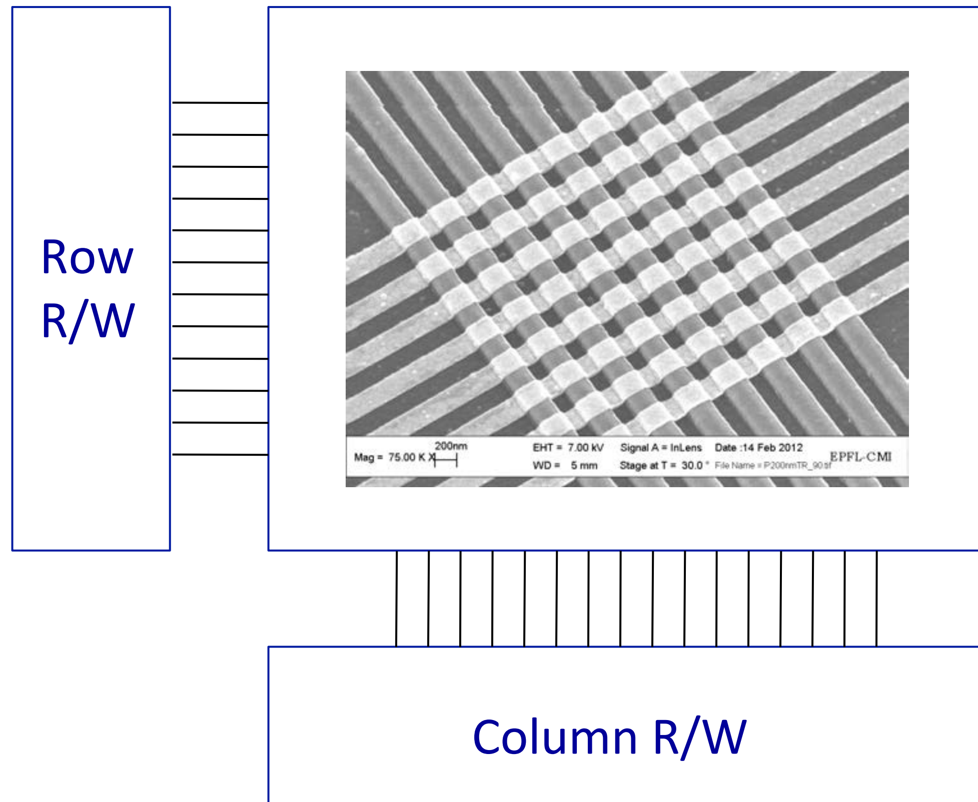
Technology Experience

- **ReRAM single cells:**
  - Fabrication from 10µm to 40nm ReRAM cells
  - 10^2 HRS/LRS ratio, 0.6 V set and -0.55 V reset voltages
  - Multiple resistance states demonstrated
  - Verilog-A modeling for the fabricated devices
- **Capability of processing single CMOS chips**
  - Chip embedding technology
- **Demonstration of two methods for ReRAM-CMOS integration for low-voltage applications:**
  - MMC-based method
  - Metal 5/6 integration

Read/Write Circuit Requirements



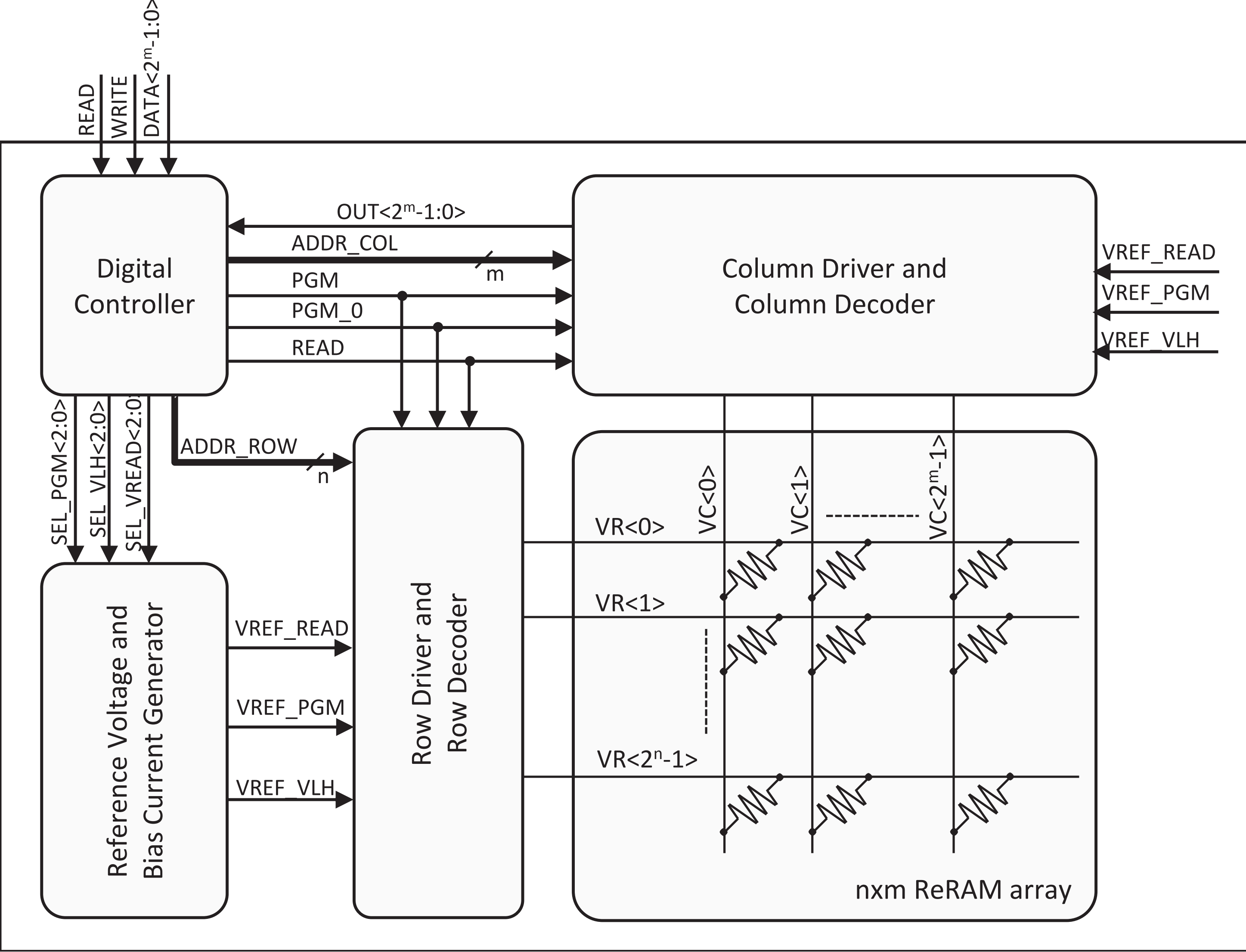
Avoid sneak-path problem

Improve noise margin at read-out

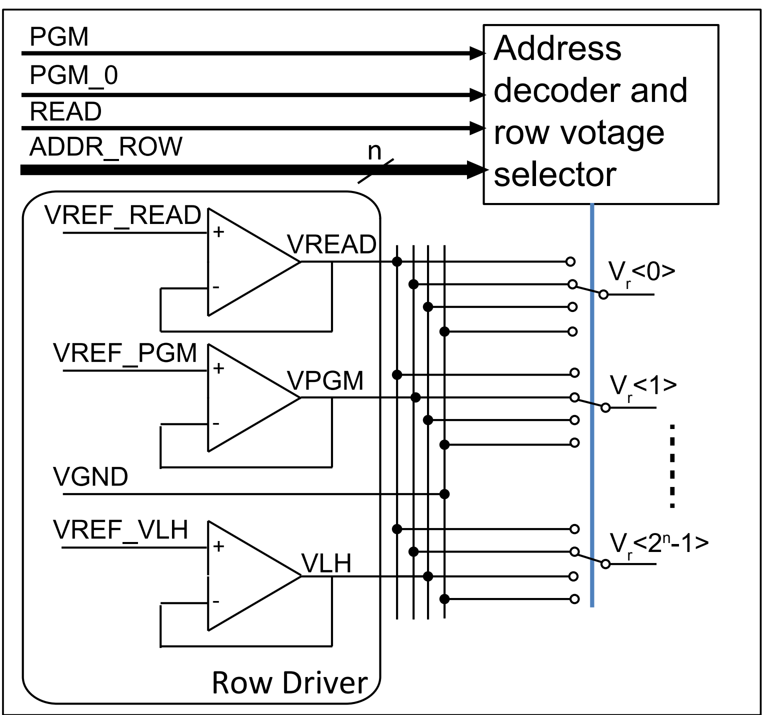
Reduce power dissipation

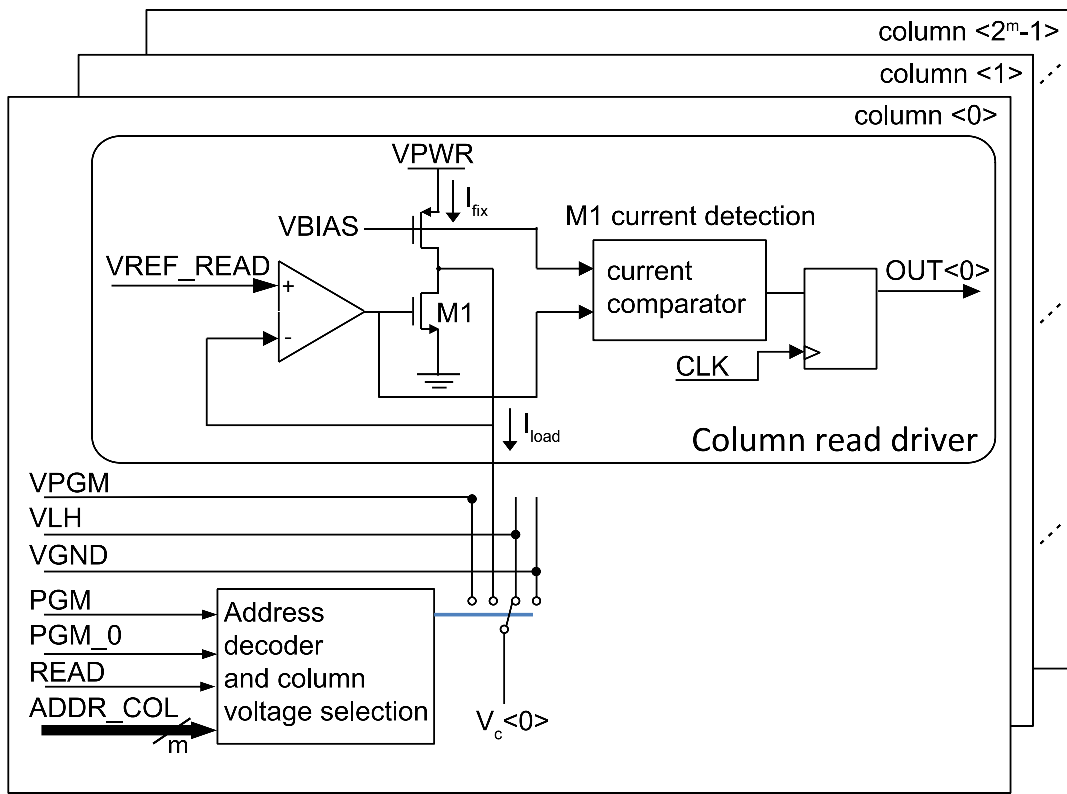
Compatible with low-voltage CMOS

Read/Write Circuit: Block Diagram



Row/Column decoders and drivers

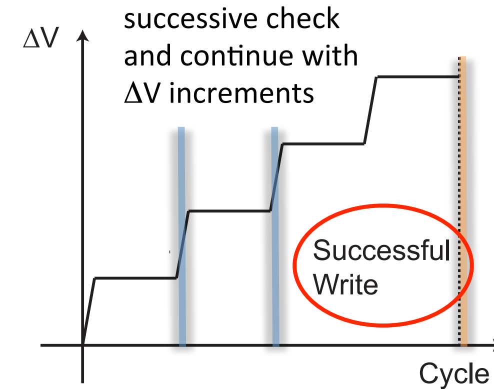


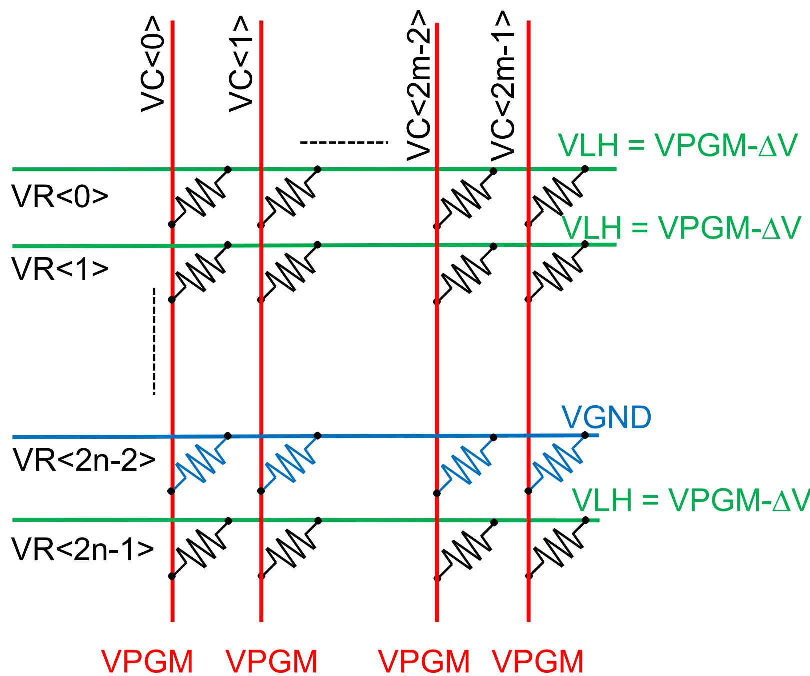


- **Row drivers**
- **Column readout amplifiers**

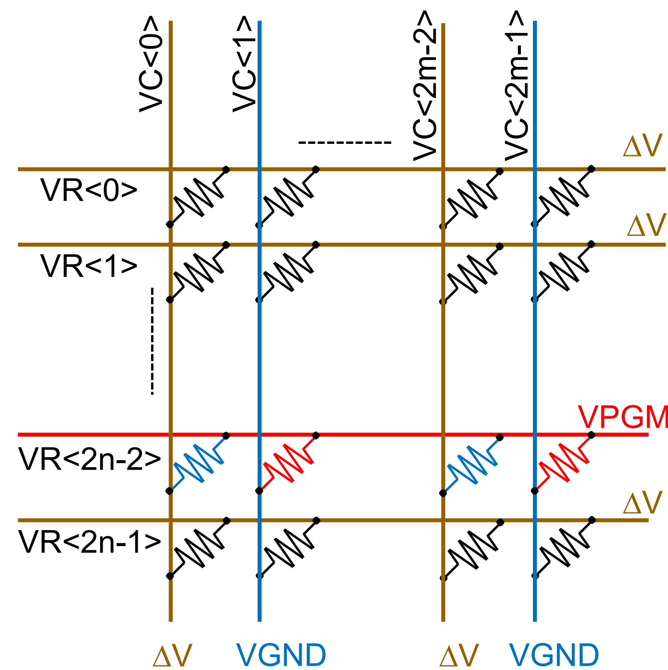
Iterative Write Strategy

- **Preliminary cell value read verification**
- **Adjustable VPGM and VLH voltages**
- **Voltage value storage for fast write**

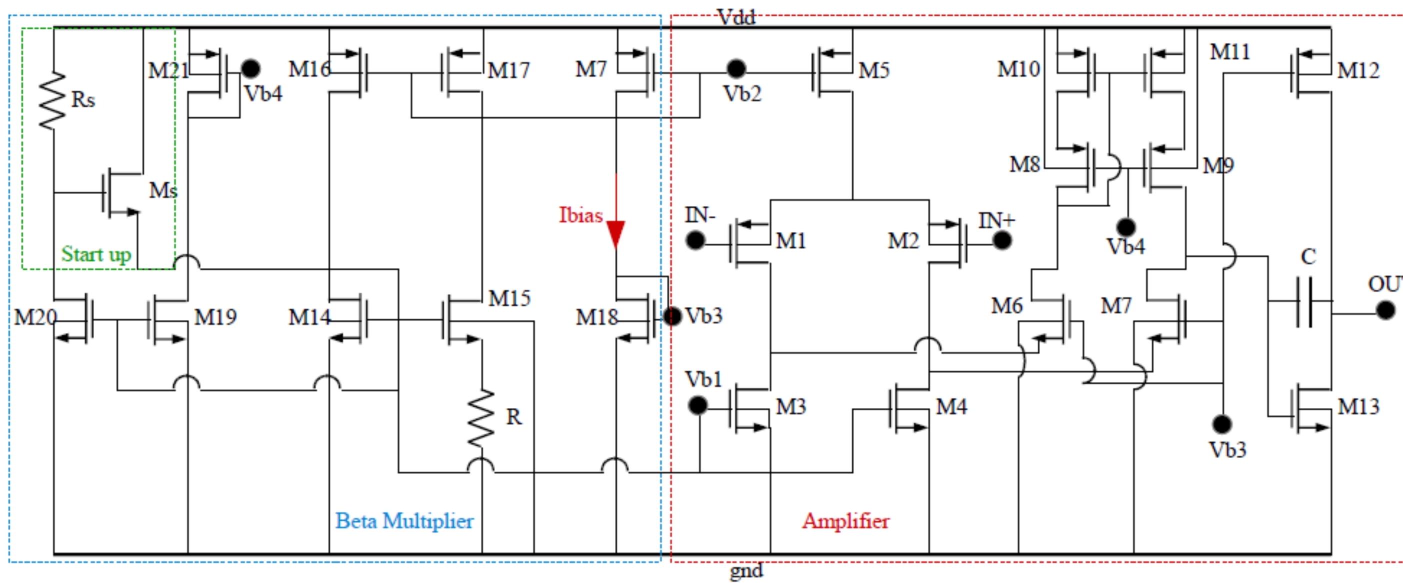




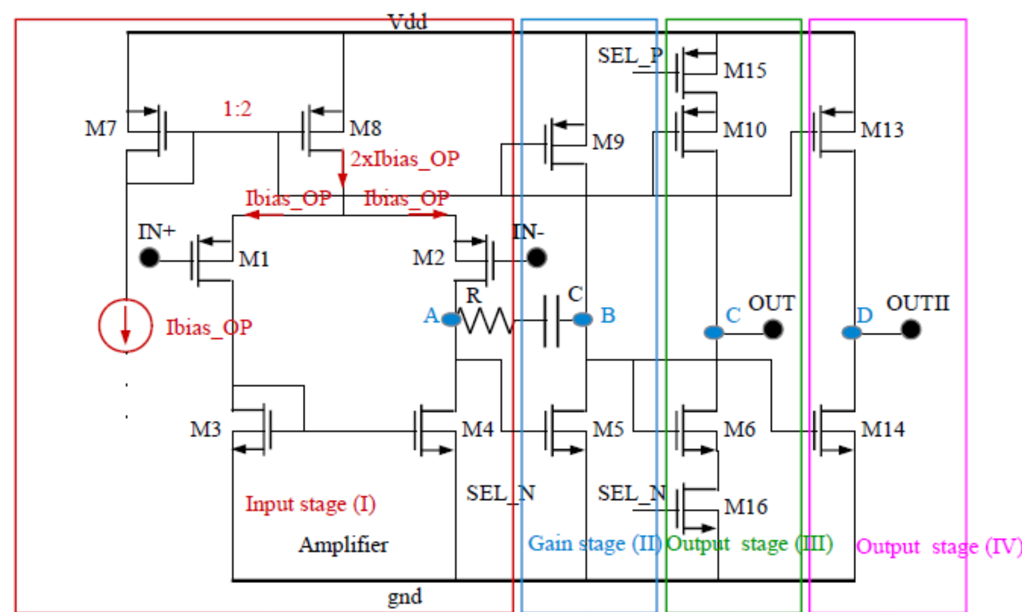
HRS programming



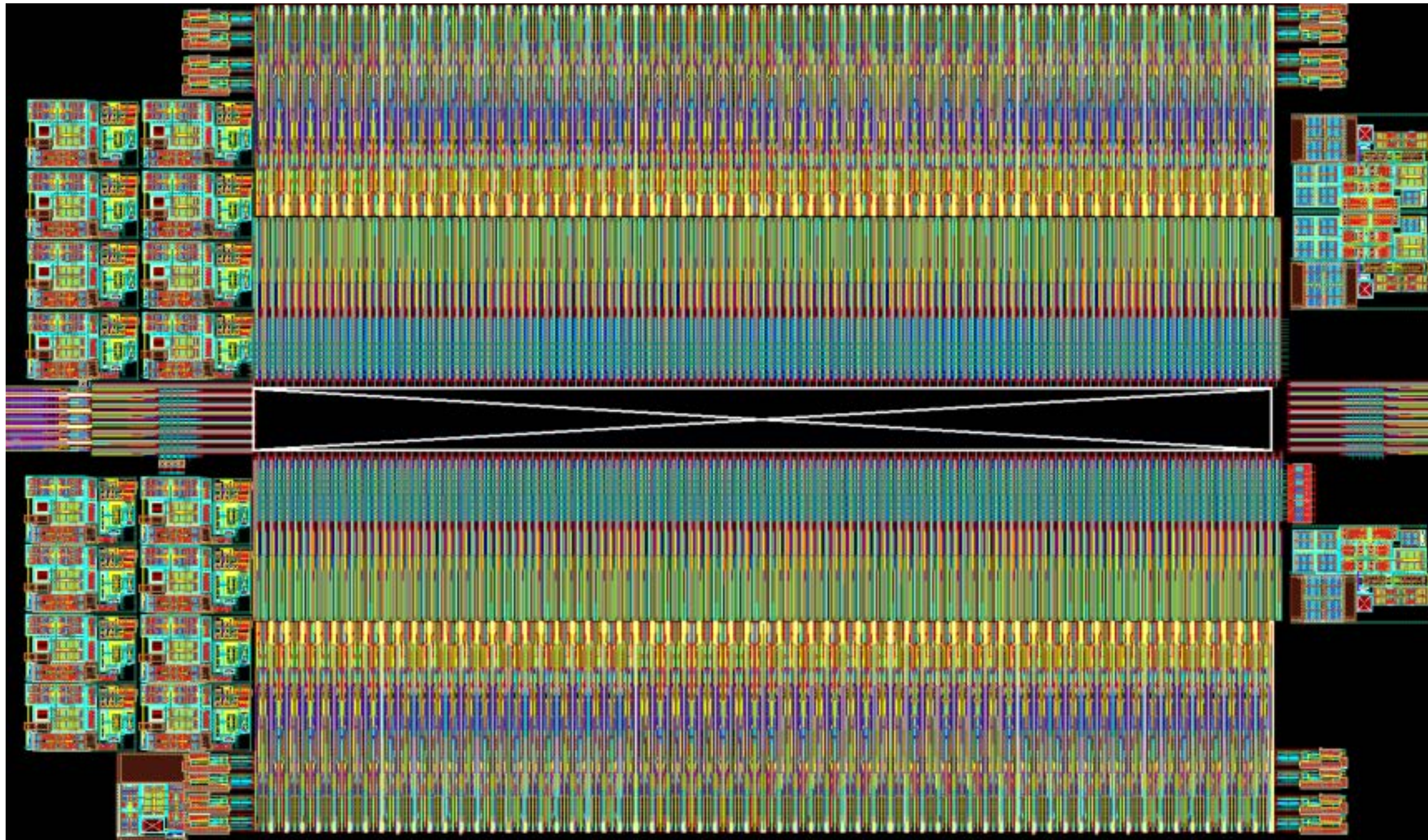
LRS programming



Bias generator + Write driver



Column read amplifier



256 x 16 bit (4 kb) transistor-less cross-bar possible

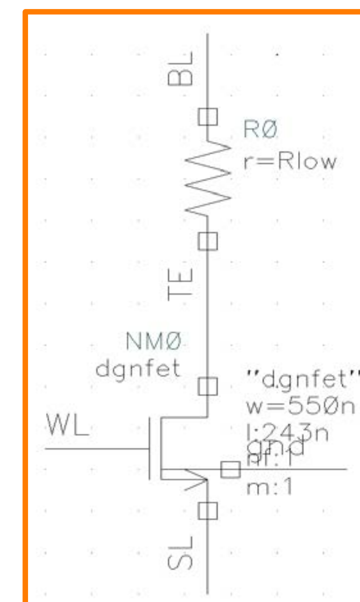
Read latency: 150 ns

Write latency: 450 ns

Capable of operating at 120° C and ±20% parameter variation

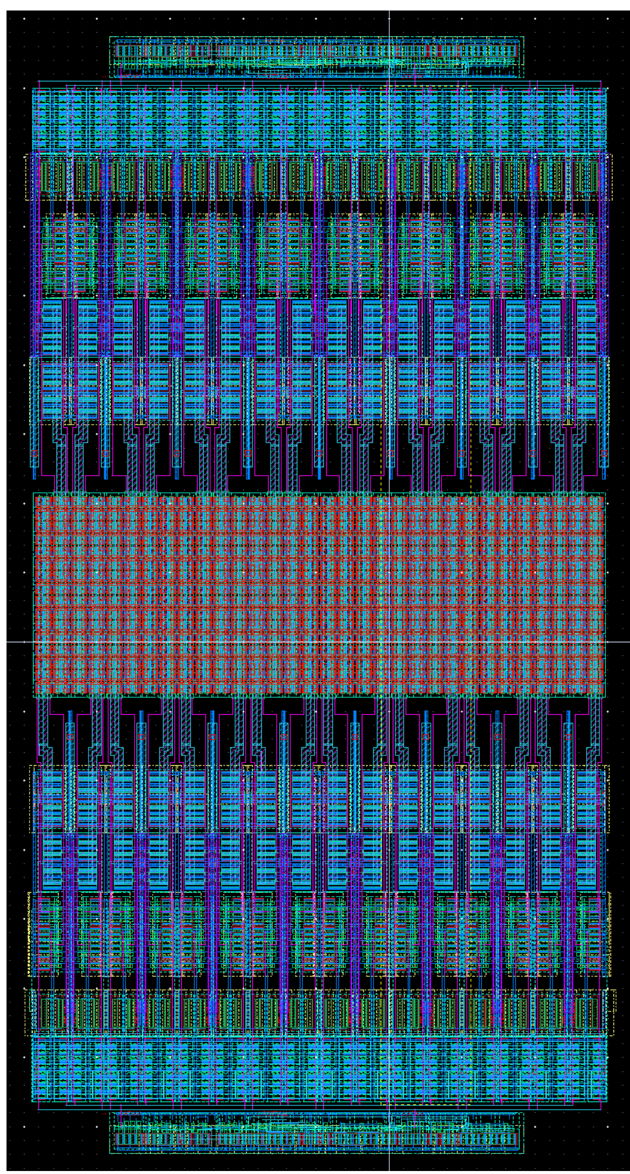
Write buffer power dissipation < 100μW

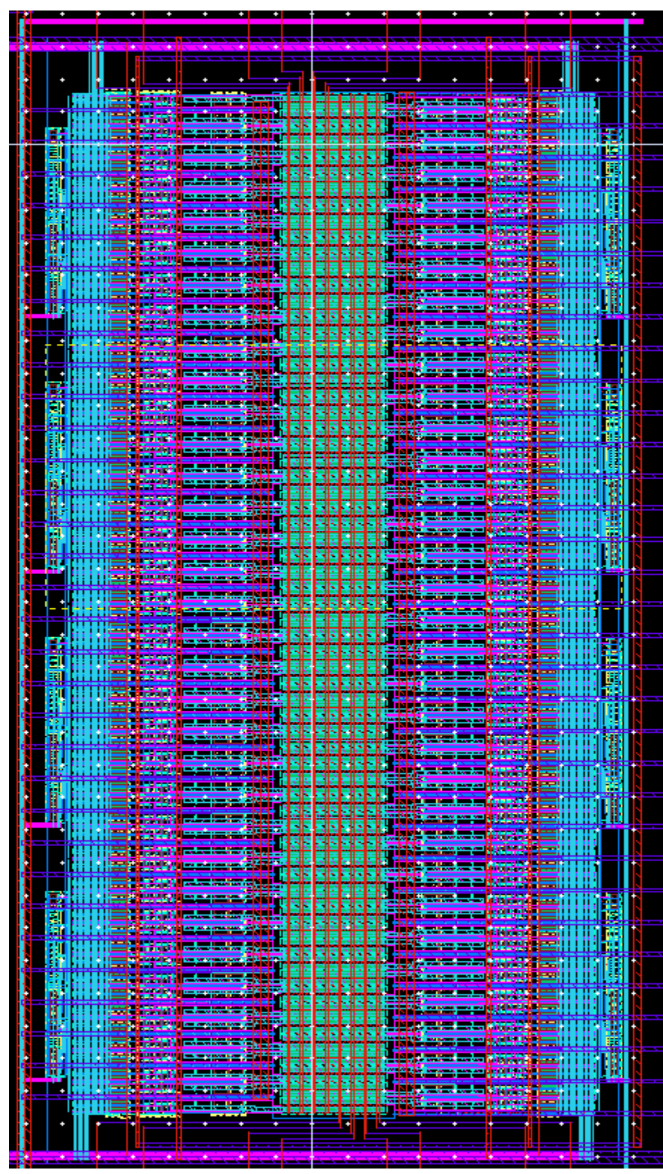
1T1R Array for Robustness

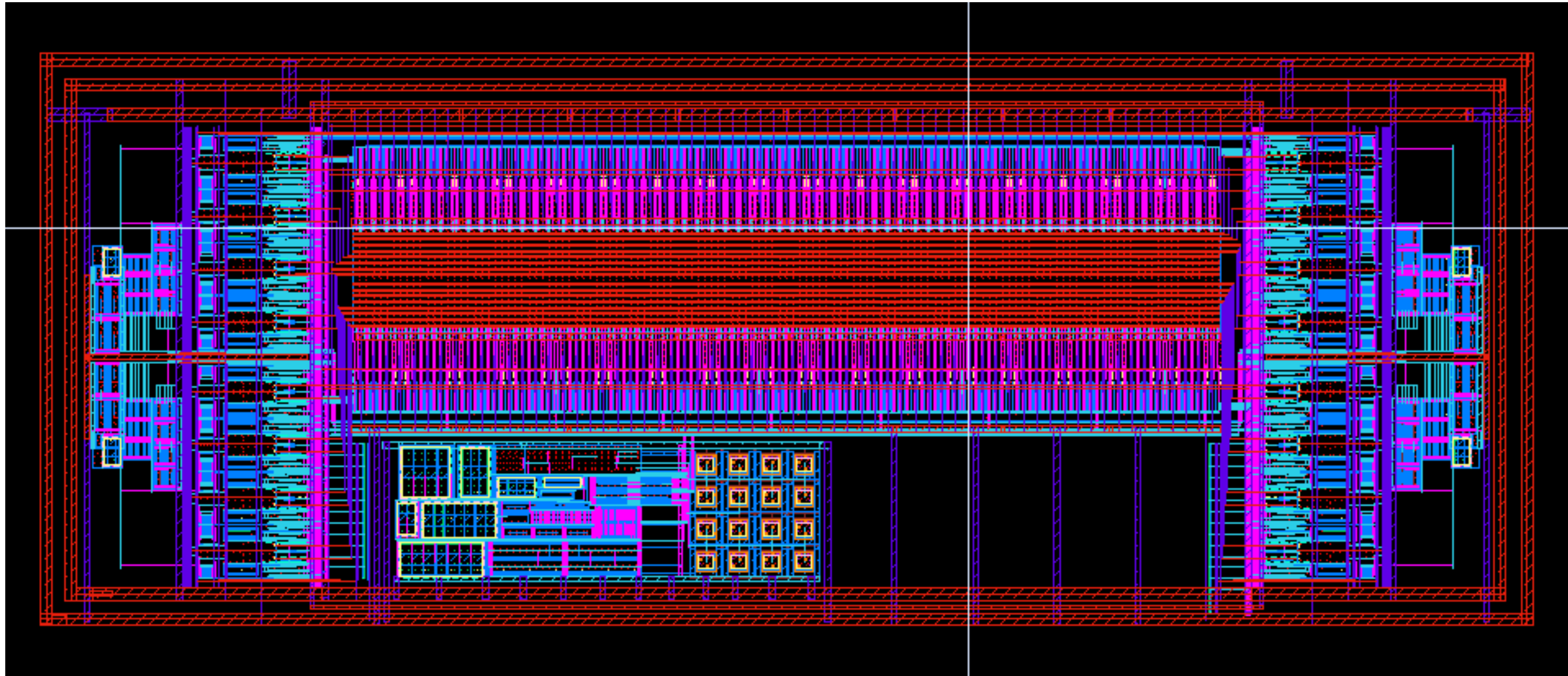


1T1R Array Implemented in 40nm CMOS technology

Test Circuit Blocks







512 x 32 bit (16 kb) 1T1R cross-bar

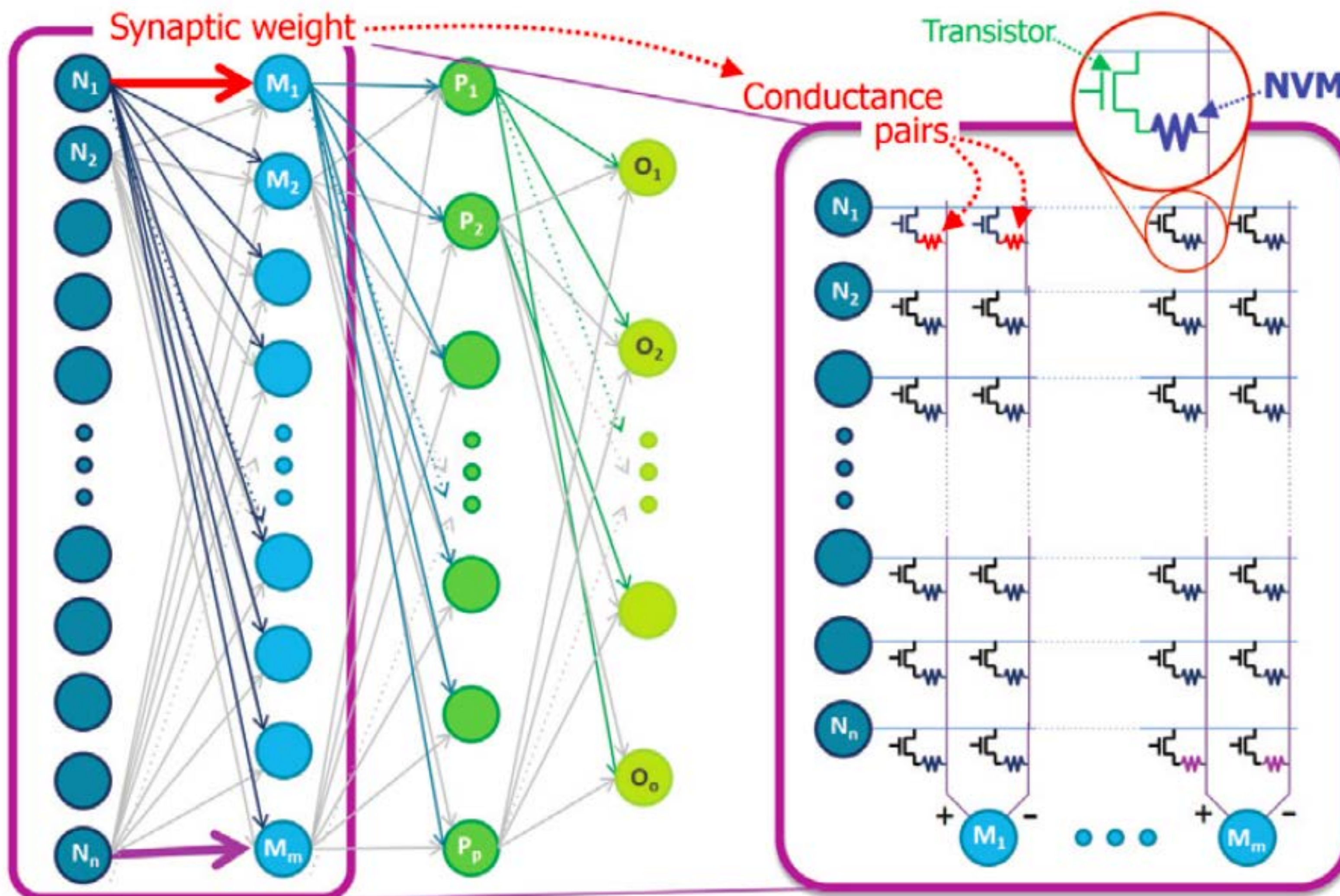
HRS = 800 kΩ

LRS = 100 kΩ

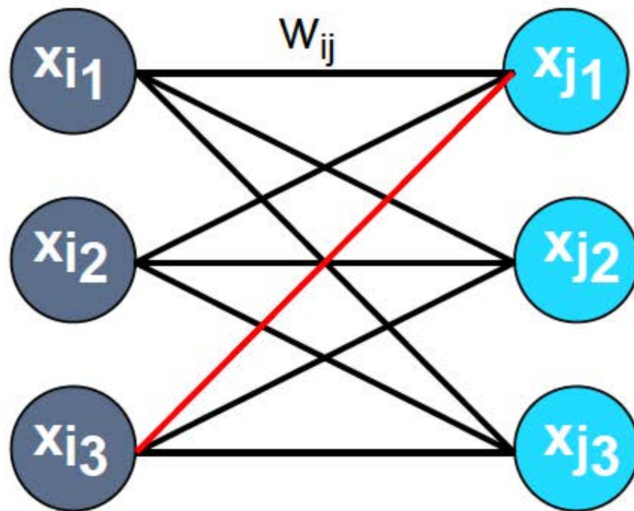
Read latency < 10 ns

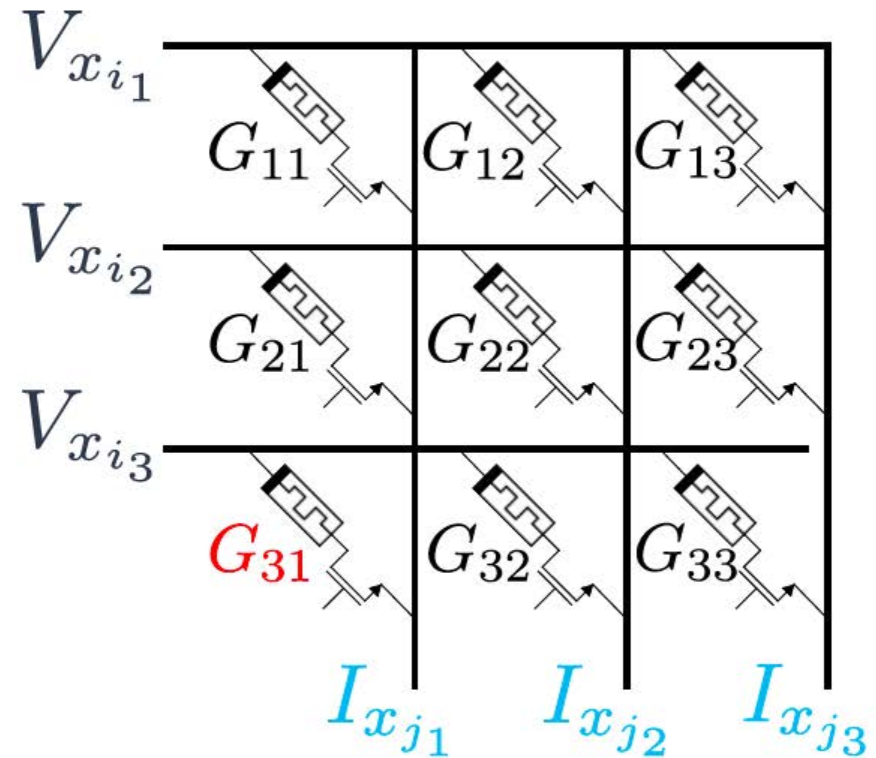
Capable of operating at 120° C and ±20% parameter variation

Neuromorphic Applications



Memristive Cross-Bar Array Implementing Weight Connections Between Two Consecutive Layers





Need the ability to change/modify the resistance values with applied voltage pulses !

Thank You !